JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

College of Engineering Pulivendula

B.Tech (EEE)– IV-I Sem

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DIGITAL ELECTRONICS AND LOGIC DESIGN

Course Objectives:

- To teach significance of number systems, conversions, binary codes and functionality of logic gates.
- To discuss different simplification methods for minimizing Boolean functions.
- To impart knowledge on operation, characteristics and various configurations of TTL and CMOS logic families.
- To outline procedures for the analysis and design of combinational and sequential logic circuits.
- To introduce programmable logic devices.

Unit I

Number Systems and Codes: Decimal, Binary, Octal, and Hexa-decimal number systems and their conversions, ASCII code, Excess -3 codes, Gray code.
Binary codes Classification, Error detection and correction – Parity generators and checkers – Fixed point and floating-point arithmetic.
Boolean Algebra& Logic Gates: Boolean operations, Boolean functions, Algebraic manipulations, Min-terms and Maxterms, Sum-of-products and Product-of-sum representations, Two-input logic gates, NAND /NOR implementations.
Minimization of Boolean Functions: Karnaughmap, Don't-care conditions, Prime implicants, Minimization of functions using Quine-McClusky method.

Unit Outcomes:

- Summarize advantages of using different number systems. (L2)
- Explain usefulness of different coding schemes and functionality of logic gates. (L2)
- Apply basic laws and De Morgan's theorems to simplify Booleanexpressions. (L3)
- Compare K- Map and Q-M methods of minimizing logic functions. (L5)

Unit II

Combinational Circuits: Introduction, Analysis of combinational circuits, Design Procedure– Binary Adder-Subtractor, Decimal Adder, Multiplier, Comparator, Code Converters, Encoders, Decoders, Multiplexers, Demultiplexers, Illustrative examples.
Sequential Circuits-1: Introduction, Latches –RS latch and JK latch, Flip-flops-RS, JK, T and D flip flops, Master-slave flip flops, Edge-triggered flip-flops, Flip-flop conversions.

Unit Outcomes:

- Apply Boolean algebra for describing combinational digital circuits. (L2)
- Analyze standard combinational circuits such as adders, subtractors, multipliers, comparators etc. (L4)
- Design various Combinational logic circuits. (L4)
- Implement logic functions with decoders and multiplexers. (L5)

Unit III

Sequential Circuits-2: Analysis and Design of Synchronous Sequential Circuits: Moore and Mealy machine models, State Equations, State Table, State diagram, State reduction & assignment, Synthesis using flip flops, Elements of Design style, Top–down design, Algorithmic state Machines (ASM), ASM chart notations.
Registers and Counters: Registers, shift registers, Ripple counters, Synchronous counters, Modulus-n Counter, Ring counter, Johnson counter, Up-Down counter.

Unit Outcomes:

- Describe behaviour of Flip-Flops and Latches.(L2)
- Compare Moore and Mealy machine models.(L5)
- Design synchronous sequential circuits using flip flops and construct digital systems using components such as registers and counters (L4)
- Utilize concepts of state and state transition for analysis and design of sequential circuits (L3)

Unit IV

Memory and Programmable Logic: RAM, Types of Memories, Memory decoding, ROM, Types of ROM, Programmable Logic Devices (PLDs): Basic concepts, PROM as PLD, Programmable Array Logic (PAL) and Programmable Logic Array (PLA), Design of combinational and sequential circuits using PLDs.

Unit Outcomes:

- Define RAM, ROM, PROM, EPROM and PLDs. (L1)
- Describe functional differences between different types of RAM & ROM. (L2)
- Compare different types of Programmable Logic Devices. (L5)
- Design simple digital systems using PLDs. (L4)

Unit V

Digital Logic Families: Unipolar and Bipolar Logic Families, Transistor-Transistor Logic (TTL): Operation of TTL, Current sink logic, TTL with active pull up, TTL with open collector output, Shockley TTL, TTL characteristics, I^2L, ECL logic Families.

CMOS: CMOS Inverter, CMOS characteristics, CMOS configurations - Wired Logic, Open drain outputs, Interfacing: TTL to CMOS and CMOS to TTL, Tristate Logic, Characteristics of Digital ICs: Speed, power dissipation, figure of merit, fan-out, Current and voltage parameters, Noise immunity, operating temperature range, power supply requirements.

Unit Outcomes:

- Summarize significance of various TTL , I^2L, ECL and CMOS subfamilies. (L2)
- Examine Interface aspects of TTL & CMOS logic families. (L5)
- Explain characteristics of digital ICs such as speed, power dissipation, figure of merit, fan-out, noise immunity etc. (L2)
- Compare bipolar and MOS logic families. (L5)

Course Outcomes:

After completion of the course, student will be able to

CO1: Understand various number systems, error detecting, correcting binary codes, logic families, combinational and sequential circuits. (L1)

CO2: Apply Boolean laws, k-map and Q-M methods to minimize switching functions. Also describe the various performance metrics for logic families. (L2)

CO3: Design combinational and sequential logic circuits. (L4)

CO4: Compare different types of Programmable logic devices and logic families. (L5)

TEXTBOOKS:

1. M. Morris Mano and Michael D. Ciletti, "Digital Design", 4th Edition Pearson Education, 2013.
2. Z. Kohavi and N. K. Jha, "Switching and Finite Automata Theory", Third Edition, Tata McGraw Hill, 2010.
3. R. P. Jain, "Modern Digital Electronics", 4th edition, McGraw Hill Education , India Private Limited, 2012.

REFERENCES:

1. J.F Wakerly, "Digital Design: Principles and Practices", 4th Edition, Pearson India, 2008.
2. Charles H Roth (Jr) and Larry L. Kinney, "Fundamentals of Logic Design", 5th Edition Cengage Learning India Edition, , 2010.
3. John.M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2006.